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New On-Board DC Power Distribution Architecture Optimized for Performance, Simplicity and Cost

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Two-stage power conversion is becoming a new standard for on-board power delivery in various networking, communications and high-end computing systems. Traditionally, multiple isolated bricks were used to power various low voltage loads on the board. In the new approach, each system board has a single isolated dc-dc converter that is used to convert nominal 48V input into a tightly regulated intermediate bus voltage. Multiple non-isolated POL converters are then used to power various loads on the motherboard from the intermediate bus.

Meeting the wide variety of continuously changing power rail requirements on different boards is much more simple with non-isolated point-of-load converters than with multiple full-featured isolated brick. This simplicity, along with lower cost, is the most significant benefit of the described two-stage, on-board power conversion.

However, in order to maximize performance (thru-put efficiency and power density) of the two-stage approach, each stage has to be carefully optimized. The most effective way to maximize the efficiency of the first stage (isolated converter) is to run it open loop with 50% duty cycle. In this case, 6V to 10V intermediate bus voltage can be generated from 36 to 60V input voltage range (ETSI spec at interface "A"). This is the most suitable intermediate voltage range for new generation of non-isolated POL converters.

In this paper, benefits of using open loop bus converters to create the intermediate bus will be discussed and compared against the traditional single-stage approach, and against the two-stage approach that uses tightly-regulated isolated converter. Two novel primary side controller ICs will be introduced that enable simple and scalable half-bridge and full bridge isolated dc-dc bus converters. Both controllers combine free-running 50% duty cycle oscillator with one or two 100V half-bridge drivers to deliver complete primary side control and drive solution in a minimal package. The controller's switching frequency and dead time between the low side and high side pulses can be adjusted to fit various applications, and power levels, and gate drive capability is optimized for, and in conjunction with, new generation of low charge power MOSFETs

To demonstrate the capability of the new architecture and controller ICs, half-bridge isolated bus converters with self-driven secondary synchronous rectification was designed. The converter delivers 150W at 8V output from 48V input with 96.5% full-load efficiency and 90W/in^2 (270W/in^3) power density. Details of the controller and circuit design will be presented in the final paper.

It will be shown how typical features of the most popular hot swap controllers can be used in conjunction with dc bus converter to further optimize system cost and reliability. Furthermore, lossless power sequencing, enabled by two-stage power conversion, will be presented and demonstrated with new generation POL converters.

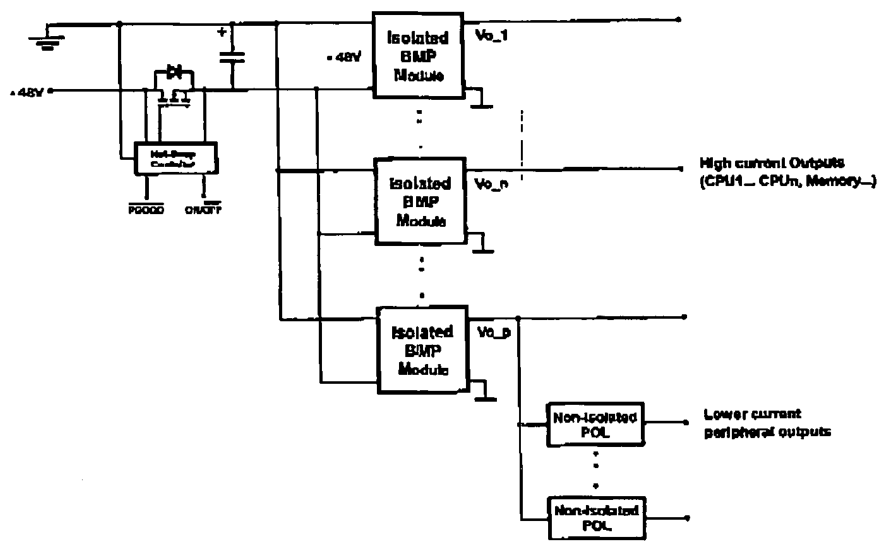


Figure 1.: Traditional on-board power distribution.

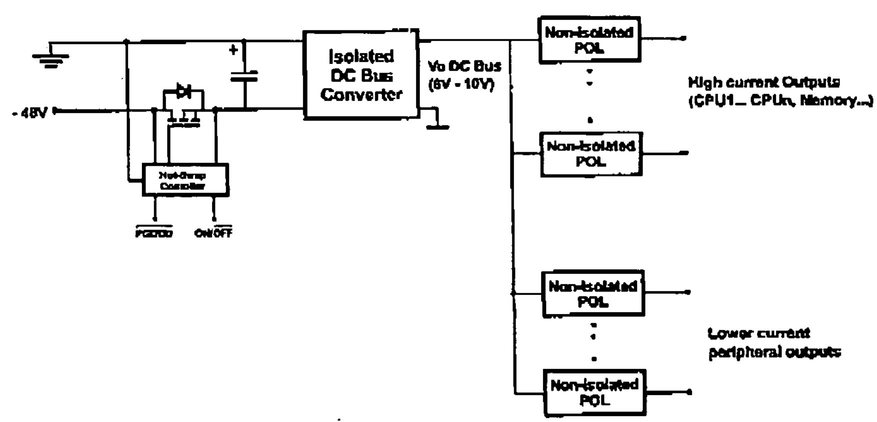
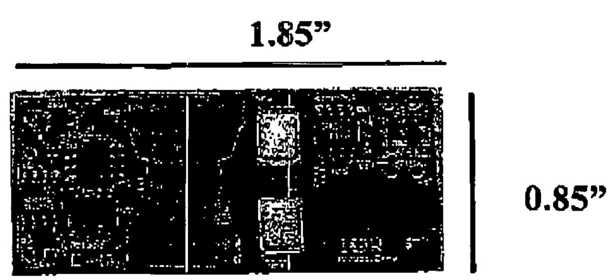


Figure 2.: Proposed on-board power distribution optimized for performance and simplicity.



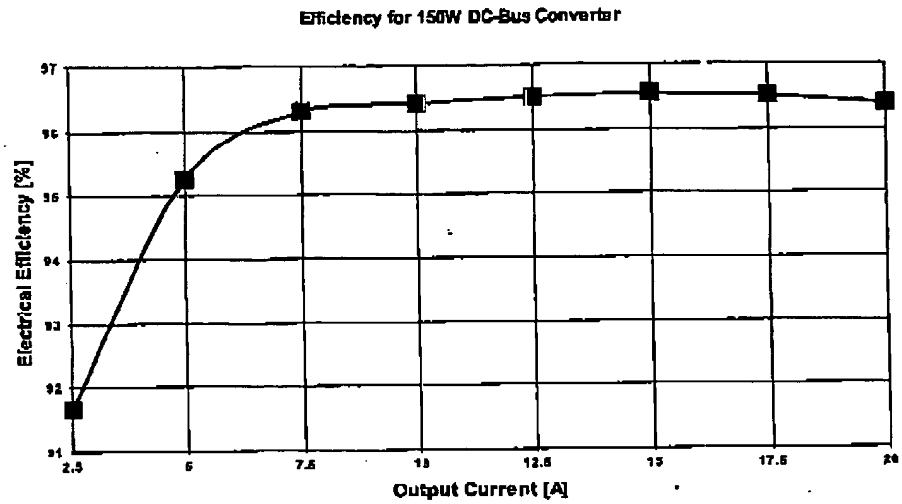


Figure 3.: Photo of the isolated dc bus converter demo board.

Figure 4.: Efficiency of the isolated dc bus converter demo board at 48Vin, 8Vout.